

WE CLAIM:

1. An apparatus for detecting a fault condition in a differential signal having a valid common-mode voltage, comprising:

an input buffer circuit that is arranged to produce a first buffered signal and
5 second buffered signal in response to the differential signal;

a first comparator circuit that is arranged to produce a first signal in response to the first buffered signal and a first reference signal;

a second comparator circuit that is arranged to produce a second signal in response to a second buffered signal and second reference signal; and

10 an output circuit that is arranged to produce a fault detection signal in response to the first signal and the second signal, whereby the fault detection signal indicates the fault condition that is due to at least one of a short condition, an open condition, and a termination by abnormal means.

2. An apparatus as in Claim 1, wherein the first reference signal and the second
15 reference signal are the same.

3. An apparatus as in Claim 1, further comprising an integrator that is arranged to provide a first integrated signal in response to the first buffered signal, and the first comparator circuit is arranged to produce the first signal in response to the first integrated signal and the first reference signal, whereby the integrator operates as a speed trap.

20 4. An apparatus as in Claim 3, wherein the integrator includes a level shifter circuit and a capacitance circuit, the level shifter providing isolation between the input buffer circuit and the capacitance circuit, and the capacitance circuit is arranged to average the first buffered signal.

25 5. A method for detecting a fault condition in a differential signal having a valid common-mode voltage, the method comprising:

producing a first buffered signal and a second buffered signal in response to the differential signal;

generating a first signal when the amplitude of the first buffered signal meets a first predetermined criteria;

generating a second signal when the amplitude of the second buffered signal meets a second predetermined criteria; and

5 producing a fault detection signal in response to the first signal and the second signal, wherein the fault detection signal indicates the fault condition when the amplitude of the differential signal is below a predetermined amplitude level.

6. A method as in Claim 5, wherein the first predetermined criteria is the same as the second predetermined criteria.

10 7. A method as in Claim 5, wherein the first predetermined criteria corresponds to the first buffered signal being below a predetermined signal level.

8. A method as in Claim 5, wherein the first predetermined criteria corresponds to the first buffered signal being above a predetermined signal level.

15 9. A method as in Claim 5, further comprising averaging at least one of the first buffered signal and the second buffered signal with a corresponding integrator.

10. An apparatus for detecting a fault condition in a differential signal having a valid common-mode voltage, comprising:

a buffering means that is arranged to provide a first and second buffered signal in response to the differential signal;

20 a first comparison means that is arranged to produce a first signal in response to a comparison between the first buffered signal and a first reference signal;

a second comparison means that is arranged to produce a second signal in response to a comparison between the second buffered signal and second reference signal; and

25 an output means that is arranged to produce a fault detection signal in response to the first signal and the second signal, such that the fault detection signal indicates the fault condition that is due to at least one of a short condition, an open condition, and a termination by abnormal means.

